

Notice of References Cited

Application/Control No.

09/781,492

Applicant(s)/Patent Under
Reexamination
ABADIR ET AL.

Examiner

A. M. Thompson

Art Unit

2825

Page 1 of 3

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,675,728	10-1997	Kunda et al.	714/28
	B	US-2002/0104065	08-2002	Tsukiyama et al.	716/6
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	EP-0697668-A1	02-1996	EUROPE	Kunda et al.	G06F 17/50
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Chang et al., VIPER: An Efficient Vigorously Sensitizable Path Extractor, Proceedings of the 30 th International Design Automation Conference, pages 112-117, July 1993.
	V	Bhadra et al., A Quick and Inexpensive Method to Identify False Critical Paths Using ATPG Techniques: An Experiment with a PowerPC Microprocessor, Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, pages 71-74, May 2000.
	W	Zeng et al., Full Chip False Timing Path Identification, IEEE Workshop on Signal Processing Systems, pages 703-711, October 2000.
	X	Zeng et al., False Timing Path Identification Using ATPG Technique and Delay-based Information, Proceedings of the 39 th Design Automation Conference, pages 562-565, June 2002.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Page 2 of 3

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	J	US-			
	K	US-			
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	M	US-			

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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Sivaraman et al., Primitive Path Delay Faults: Identification and Their Use in Timing Analysis, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, pages 1347-1362, November 2000.
	V	Lin et al., Dynamical Identification of Critical Paths for Iterative Gate Sizing, IEEE/ACM International Conference on Computer-Aided Design, pages 481-484, November 1994.
	W	Zeng et al., Full Chip False Timing Path Identification: Applications to the PowerPC Microprocessors, 2001 Proceedings of Design, Automation and Test in Europe, pages 514-518, March 2001.
	X	Wolf et al., Intervals in Software Execution Cost Analysis, 13 th International Symposium on System Synthesis, pages 130-135, September 2000.

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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Page 3 of 3

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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Raimi et al., Detecting False Timing Paths: Experiments on PowerPC microprocessors, Proceedings of the 36 th ACM/IEEE Conference on Design Automation, pages 737-741, June 1999.
	V	
	W	
	X	

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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.